To: John D'Auria

From: Joel Rogers

Re: DAQ Electronics' Final Drawing

Introduction

I have just completed the "as built" drawing of the NIM and Camac electronics for DRAGON(cf. pg.10). This memo provides information which will be useful if it becomes necessary to modify or repair the electronics, e.g. in the case of bin failure many wires will need to be removed to take the bin to be repaired. The purpose and function of each gate, amp, discriminator, etc. is given below, but first some general comments on the design of the electronics and the layout of the drawing.

The physical position of the modules in the bins and crates is preserved in the drawing. Most wires are represented by lines, except in the case of scaler and NIM/ECL converter connections which are represented by —o and ▷ symbols. In referring to a particular electronic module, the 1st letter U, C, L, O, and E indicates that its location is in Upper-NIM, Camac, Lower-NIM, Overflow-NIM, or Eurocrate. The second field gives the slot in the bin or crate, and the final number (in parentheses) gives the sub-module position for modules with multiple sections, such as a quad-discriminator. The functions of each (sub)module is given in physical order, top to bottom inside a crate, then left to right in the crate, then top to bottom from crate to crate in the racks.

The modular electronics to be described is controlled by a DAQ computer program in midmes01 computer, located in the bottom of the TRIUMF rack near the target. The software and module specs are described in a blue binder "DRAGON Midas DAQ Guide", usually found near midmes01. The essential clients which must be running to take data are Midas Logger and Frontend, which is listed in the binder under "dragon.c". To start the software follow the instructions on the first page of the binder or midmes01:~/online/login.doc.

Events are converted by ADC/TDC's and stored in one or both of two Camac memories. When either memory fills a LAM triggers the frontend software module "dragon" which reads both memories. One memory, called the gamma-memory, receives conversions from the gamma array. The other memory, called the H-(for heavy ion)memory, receives the conversions from the end-detector and elastic monitor detectors. These latter 2 events are uncorrelated and low-rate, so the H-memory records both as needed. Singles events correspond to one particle detected in the elastic detector, gamma array, or end-detector. A forth type of event, the coincidence detection of gamma and heavy-ion, is recognized in the frontend software from the pattern of matching TDC signals, one from the gamma-TDC and one from the end-detector TDC. Coincidence events are assembled in the frontend software by copying the 2 pieces of the event from gamma- and H-memories.

A main function of the electronics is to control access to the ADC's and TDC's so that the dead time is the same for the two pieces of the coincidence events. Whenever either gamma or H-detector converters become busy, an inhibit signal is generated which prevents both gamma- and H-detector electronics from processing a second event until the first event has entered one or both memories. Following each gamma detection, the H-detector converters are kept live for 10 microseconds(us), the maximum valid flight time of a heavy-ion. Following the 10 us waiting period, both gamma and H-detector converters become dead until all ADC's and TDC's have finished converting and transferred their conversions to one or both memories. By

forcing the two detectors to be dead for the same periods following each single- or coincidence-event, the possibility of fragmenting coincidence events due to singles' dead-time is avoided.

Each Module's Function

U1(1) - LRS821Z quad discriminator "Front Stretch" receives the OR of the output of 16 leading edge discriminators qualifying the front DSSSD strips. Thus each DSSSD event is counted once even if it has several struck strips. The output drives scalers and end-detector acquisition through "End Det. Fanin" gate at U4(2).

U1(2) - LRS821Z quad discriminator "Sum LED" receives the wired-OR of 30 leading-edge discriminators connected to each of the gamma array detectors. The output goes to scaler-8, which therefore measures the gamma singles rate.

U1(3) - LRS821Z quad discriminator "EL LED" measures the leading edge time of the elastic monitor signal for the purpose of pulse-shape-discrimination (PSD). The threshold (61mV) was determined empirically to match the CFD threshold in the discriminator at L6.

U1(4) - LRS821Z quad discriminator "END Fan Out" generates a 1.1 us pulse at the trailing edge of the "Busy" pulse from U6(3). This end-pulse goes to CLI of C11/22 to clear ADC/TDC's at the end of the transfer of an event to Camac memories. The width of the output must be long enough to insure that the LRS4300B ADC's have reset to zero before allowing the next event through the "RUN" gates at U5(1) and U5(3).

U2(1) - LRS465 "PSD GATE"'s output width (=300ns) sets the coincidence time required between the elastics' LED and CFD discriminators at the input to the "EL Retime" gate (below). The complementary output triggers HI-TDC27 at the trailing edge of the 300ns window, allowing PSD to be refined offline. See my 1-Dec-03 memo ~/online/elasticpsd.doc for a description of the elastic PSD conceptual design.

U2(2) - LRS465 "EL Retime" gate establishes the 300ns coincidence between elastics' discriminators while maintaining the time of the CFD at its output.

U2(3) - LRS465 "r.f. FANOUT" regenerates the signal from rack 7A which contains the fiber-optic receiver from the low-beta buncher of ISAC. This periodic 11 MHz pulse is distributed to separate gamma- and H-retime gates at U3(2) and U3(3).

U3(1) - LRS622 "gamma-clip" regenerates the gamma time pulse to have width 200 ns for triggering the ratemeter at O6.

U3(2) - LRS622 "gamma.rf" passes the first 2 or 3 r.f. pulses following the gamma CFD time. These pulses cause 2 or 3 successive conversions in the gamma TDC, giving a choice of two different r.f. phases in the analysis.

U3(3) - LRS622 "H.rf" passes the first 2 or 3 r.f. pulses following the H discriminator time. These pulses cause 2 or 3 successive conversions in the H TDC.

U3(4) - LRS622 "H Clip" fans in the two sources of H triggers, elastics and end-detector. The 200ns output width sent to the above gate is comfortably wider than 2 r.f. cycles.

U4(1) - LRS429A "gamma fanin" regenerates the 200ns input from U3(1). A 1ns shorted stub clips the output to the "gamma run" gate at U5(1) so that no pulse-width ambiguity occurs in the eventual gamma ADC/TDC trigger.

U4(2) - LRS429A "END DET. FANIN" combines and fans out the two possible sources of end-detector discriminator pulses. The "A6" input from the ion chamber(i.c.) is normally open since the i.c. is rarely used.

U4(3) - LRS429A spare

U4(4) - LRS429A "H FANIN" regenerates 200ns pulses from U3(4). A shorted stub clips the output to the H "run" gate at U5(4) to eliminate pulse-width ambiguity.

U5(1) - LRS465 "gamma RUN" gate passes the clipped gamma trigger pulse if none of 3 possible inhibit conditions exist. The sources of inhibits are the conversion "busy or CLI" from U8(1), memory read busy from C13(5), or DAQ stopped (= Camac Inhibit) from C13(2).

U5(2) - LRS465 "gamma to H veto" AND's the two sources of veto from the gamma array which form part of the inhibit for the H "run" gate at U5(3). Instead of being inhibited for the full duration of gamma readin, the first 9.5 us of the inhibit are canceled by the complementary signal from gamma "hcoinc" gate at C5(2). Canceling the veto to H "run" allows H trigger pulses to pass through the H "run" gate for 9.5 us following each gamma trigger, comfortably shorter than the full-scale (10us) of the gamma and H TDC's.

U5(3) - LRS465 "H RUN" gate passes clipped H trigger pulses if none of 3 possible inhibit conditions exist. The sources of inhibits are the above veto from U5(2), memory read busy from C13(7), and DAQ stopped from C13(3).

U6(1) - LRS429A "gamma fanout" distributes the gamma "run" gate logic pulse to Camac scaler and to start the gamma adc gate generator at C5(1). The output width 200ns is also appropriate for selecting 2 or 3 r.f. pulses at U3(2).

U6(2) - LRS429A "hcoinc fanout" regenerates the 9.5 us wide signal from C5(2) which sets the gamma/end-detector resolving time. The complementary output is clipped by shorted stub form a narrow pulse at the end of the 9.5 us which is sent to start the gate at U8(2).

U6(3) - LRS249A "busy" OR's all primary sources of frontend busy, 2 from gamma side and 2 from H side. From each side comes RQO from the appropriate memory controllers at C11 and C22. Also from each side comes IRI(=inhibit read input) from gate generators at U7(1) and U9(2), the wait times for the appropriate ADC/TDC's to convert before reading them into the memories.

U6(4) - LRS249A "H fanout" distributes the H "run" logic pulse to various destinations.

U7(1) - LRS222 "hcoinc stretch" starts at the end of the 9.5 us end-detector coincidence time and runs for 2us. Output goes to "gamma IRI" at U8(2), making the gamma read inhibit last long enough to insure that the latest gamma TDC (from the end-detector) has finished converting before reading the gamma TDC.

U7(2) - LRS222 "HADC gate" generates a gate signal for the Silena ADC's. The width is not critical because the ADC's are peak sensing and the rate is low. Because the i.c. signals are microseconds later than the DSSSD and elastic signals, the width is selected to be 4.5 us.

U8(1) - LRS429A "busy OR CLI" forms the overlap OR of the master busy from U6(3) with the end-busy clear pulse from U1(4). The clear pulse extends the busy by its width = the time for ADC's to settle to zero counts. This extra busy width holds off the "run" gates so that a following event trigger cannot pass the "run" gates until the ADC's are ready.

U8(2) - LRS429A "gamma IRI" forms the OR combination of the end-detector resolving time with a 2 us extension to allow the gamma TDC to convert the latest stop input which might come at the end of the resolving time. When applied to the gamma memory driver's inhibit input, IRI at C11, it forces the driver to wait long enough to begin the memory transfer.

U8(3) - LRS429A "hIRI fanout" regenerates the NIM output from U9(2).

U8(4) - LRS429A "Pulser clip" cleans up a transformer inverted (IT100) TTL signal from the pulser at L2 which avoids needing a TTL/NIM converter module.

U9(1) - LRS222 "PSD delay" delays the elastic LED pulse from U1(3) to center the 300ns PSD acceptance window with the CFD pulse at gate U2(2).

U9(2) - LRS222 "hIRI generator" forms a 40 us hold-off gate to wait for the H ADC/TDC's to convert before starting readin to memory. The time is appropriate for the slower conversions of the Silena ADC's.

U10 - LRS4616 "Back ECL/NIM" converts 16 logic pulses from the back-side DSSSD strips to NIM standard logic pulses which are ORed at U11(2). Regenerated ECL outputs go also on to the H TDC inputs 0-15.

U11(1) - LRS628 "FRONT fanin" adds the 16 NIM logic levels from the front-side DSSSD strips. The output has one (or more) pulse(s) marking the time(s) of strip signals exceeding the threshold set in the amp/discriminator modules at E3.

U11(2) - LRS628 "Back fanin" adds the 16 NIM logic levels from the back-side strips to form a back trigger pulse (used only for diagnostic scope monitoring).

U12 - ECL/NIM "Front ECL/NIM" converts 16 signals from ECL to NIM for developing the end-detector trigger via linear summing at U11(1).

C1/C2 - LRS 3420 "gamma CFD" 16 channels in C1 and 14 in C2 receive anode pulses from gamma array detectors. Inputs come from RC filters following 10X amplifiers at L8, L9, L10. Outputs are individual logic pulses which go on flat-cable to gamma TDC's and also 2 OR-outputs which are combined to form input to gamma trigger at U3(1). The CFD levels are individually set from ODB variable /Equipment/gTrigger/Settings/CFD_Thresholds. The output pulse width is set in dragon.c CFD_WIDTH to place the trailing edge of the output pulses on-scale in the TDC's. Thus the output width is used as a delay to the TDC's, avoiding the need for 30 more delay cables.

C3/C4 - LRS4413 "gamma LED" 30 leading-edge discriminators receive a second signal from the same amplifiers as above CFD's, but unfiltered to provide better time resolution. Outputs go on flat cable to the first 30 inputs of a TDC at C8. All 16 thresholds are the same, set from the ODB. The scales of CFD_Thresholds and LED_Threshold are different so that the levels should be matched by making the LED rate(scaler-8) about 2X higher than CFD rate (scaler-1).

C5(1) - LRS2323A "gamma gate" triggered by gamma "run" width set by the ODB's

ADC_gate_width_ns, typically 650 (ns). This width sets the integration time of the charge sensitive gamma ADC's. The larger the width, the bigger the charge and therefore the bigger the pulse-height in the paw spectra. When the width changes, recalibration is needed (c.f. ~/online/gamma_array.doc).

C5(2) - LRS2323A "hcoinc" triggered by the output of the above gate, this width, set by HI_TOF_delay_ns, is the delay time from gamma trigger to the latest possible H trigger = maximum heavy ion TOF, which must be less than the fullscale CFD TDC range, described in C8 below. The usual setting, 9500(ns), usually allows for extra i.c. internal delays also.

C7 - LRS3377 "gamma LED" is a 32-input TDC, the first 30 channels of which receive the 30 outputs from the leading-edge-discriminators at C3 and C4. Full scale range is set from LED_TDC_range_ns.

C8 - LRS3377 "gamma CFD" receives 30 output from the CFD's at C1 and C2 and also r.f. and H-trigger on stop inputs 30 and 31, respectively. Its full scale range is set from CFD_TDC_range_ns, usually 10000.

C9/C10 - LRS4300B "gamma ADC" receives 30 inputs from the gamma array splitters via 30 individual 128ns delay cables. Each ADC has an individual pedestal memory containing a pre-loaded pedestal which is subtracted following conversion and prior to reading into Camac memory. The pedestals are written into the ADC's from /Equipment/gTrigger/Settings/Pedestals, which is itself written with pedestal calibration data (c.f. gamma_array.doc). The subtraction of pedestals may produce events in memory with TDC's but lacking ADC words. Overflow occurs at 1024 or 2048 channels, varying among different 16-channel modules.

C11 - LRS4301 "gamma MEM DRIVER" controls the transfer from gamma ADC/TDC's to Camac memory following the conversion of an event. Inputs are GAI, IRI, and CLI which provide gate/start input, input-reading-inhibit, and clear-input, respectively. These are NIM pulses which synchronize the reading and clearing of the ADC/TDC's for each event. The module produces NIM output RQO as well as several ECL output for stepping through the reading of the modules at C7-10. RQO is a NIM pulse which indicates that data is ready to be transferred to memory. It is used to hold-off the gamma "run" gate until transfer is complete. Another NIM output, WSO, is useful for checking on the proper operation of the read sequence (c.f. C22 below).

C12 - LRS4302 "gamma MEM" temporarily stores gamma events and signals the computer via LAM when it is 3/4 full (=12288 16-bit words). Since the LAM is detected in Midas by polling in Linux, a delay may occur between LAM and event service by dragon.c frontend. During this delay the memory continues to fill until it reaches 16384 words, at which point RQO closes the run gate until the memory is emptied by the frontend. Memory writing synchronization is controlled by several twisted-pair-cable signals as shown on the drawing. Synchronization between dragon.c frontend and the "run" gates is controlled by NIM output register at C13, described below.

C13 - CES1320 "NIM OUT" register provides pulses and levels I, not-I, not-busy, and beginning-of-run, which are used to control the gamma and H "run" gates and the scalers at C15-C16. The frontend software sets the levels by writing and clearing individual bits of a binary word stored in the module.

C14 - LRS2132 "HV Interface" provides computer control of the external 30 channel LRS4032A HV mainframe, via a TTY cable. The dragon.c frontend reads the present high-voltage for each gamma detector and compares it to the value tabulated in the ODB, /Equipment/gTrigger/Settings/HV. Discrepancies greater than 2v are reported via the Midas error reporting (to all clients). A separate program ~/bin/hvcontrol writes the same ODB data into the 4032A

hardware, only needed following a power outage or when changing array gains.

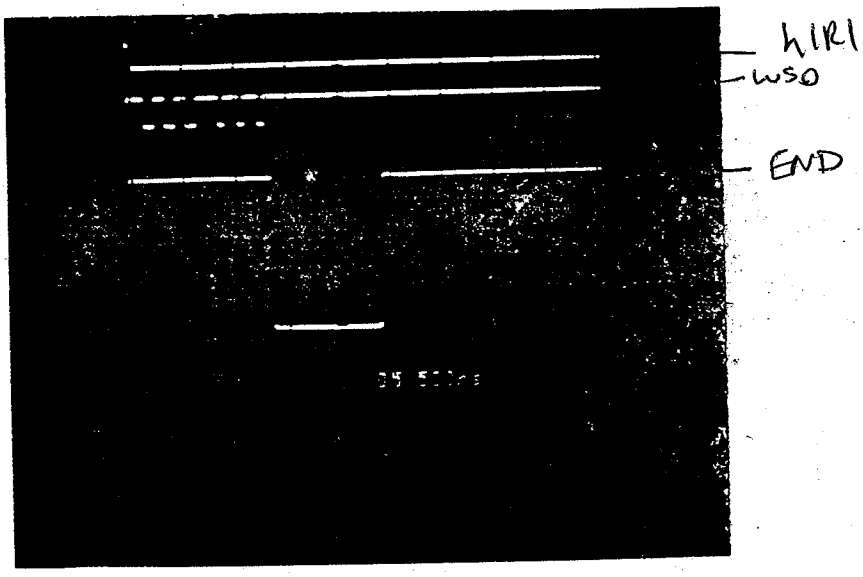
C15/C16 - KS3615 "HEX scaler" are two identical modules each containing 6 NIM pulse counters. Inputs come from various places as indicated by the -o symbols on the drawing. The 12 scalers count independently and with little dead time. The scalers are read and cleared every 1s by dragon.c and written as a separate event into the logging file. In addition the Midas Analyzer, if it is running, sums the scaler data into /Equipment/Scaler/Sums so that the total accumulated in the 12 counters is written in the final .odb file. The scalers are inhibited between runs and cleared at the beginning of each run by a pulse from the above C13 output register.

C17 - CES5170 "NIM to ECL" converter takes 7 inputs from various places in the electronics as indicated by the _> symbols on the drawing. The ECL version of each signal is used for various gamma and H TDC stops. The module is passive and so could be moved to a separate crate if more space is needed in the "C" crate.

C18 - LRS3377 "HTDC" 32 input time digitizer of which the first 16 stop channels(0-15) convert the times of the back DSSSD strips and 30/31 are r.f. and gamma-time, respectively. Stop-27 is also used for elastic PSD time.

C19/C20/C21 - Silena 4418/V "HADC" and "EL ADC" converters, 8 channels per Camac module. The peak sensing ADC's have a 1.5% zero offset set in the frontend_init routine of dragon.c. 10v fullscale = 4000 channels.

C22 - LRS4301 "HMEM Driver" operates similarly to the identical gamma module at C11 described above. Following a gate/start from U7(2), the ADC/TDC's convert and are transferred to the memory (see below) in left-to-right order in the Crate. The required event-header-word is supplied by the TDC at C18. The following photo shows the WSO output using the L2 pulser as the only event source. The top trace is the scope trigger on the trailing edge of U9 "hIRI", the middle trace = WSO, showing a NIM level pulse for each word transferred to memory, and the bottom trace = U1(4) "END" which goes to CLI of this module. The WSO pattern shows three words from the H TDC, followed by 3 words from the H ADC. The TDC words are a header and one 2-word datum. The ADC words are two header words followed by a single data word. This pattern is characteristic of an elastic pulser event without r.f., the simplest of all possible events.



C23 - LRS4302 "HMEM" memory acquires elastics and end-detector event lists and signals the DAQ computer via LAM when the level reaches 12288 16-bit words. In the Analyzer software module hicalib.c, elastic detector events are recognized by the absence of any of the 16 conversions from C19 and C20 ADC's. This gives the DSSSD events priority over the elastic events in case both should occur in the same ADC gate; this would only occur in case of a high (noise) rate in the DSSSD, which should be eliminated by suitable choice of threshold at E3, described below.

L2 - Ortec688AL "1Hz pulser" optionally sends a shaped pulse to the "test" input of the Canberra 2003B preamp. The rate may be set at 0, ~1 or 60Hz using the central front panel switch.

L4 - Ortec460 "Shaping amp" forms unipolar and bipolar pulses from the elastics preamp. The unipolar goes to an ADC and the bipolar goes to a constant-fraction-discriminator at L6, described below.

L5 - Ortec451 "Timing filter amp" forms a 20ns-differentiated version of the elastics using a T-split signal from the preamp. This signal preserves the rise-time difference between elastic detections and noise in the elastic detector, to facilitate pulse-shape-discrimination by CFD/LED time difference.

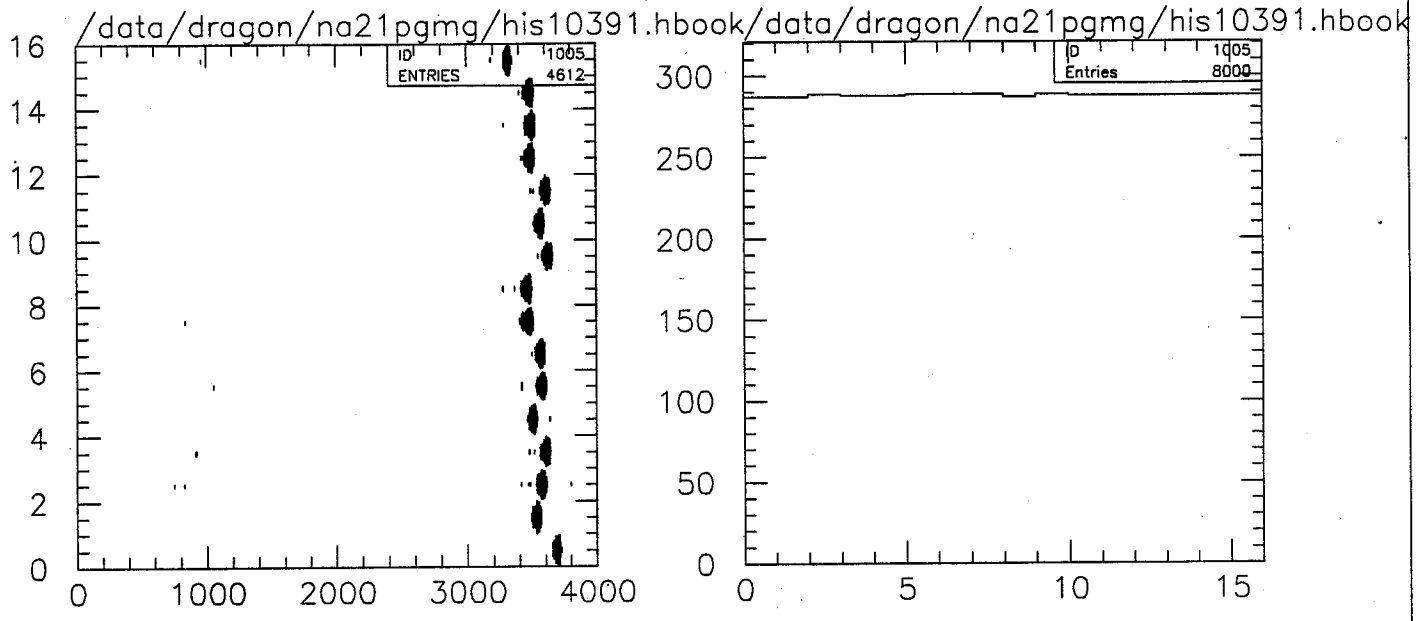
L6 - TC241 "Timing SCA" constant-fraction-discriminator shapes the signal from the elastics' shaping amplifier and sets a threshold at 1/10 the full-scale pulser signal, approximately 0.9 on the front panel "E" pot. The same pulser signal is used to set the LED threshold at U1(3), described above.

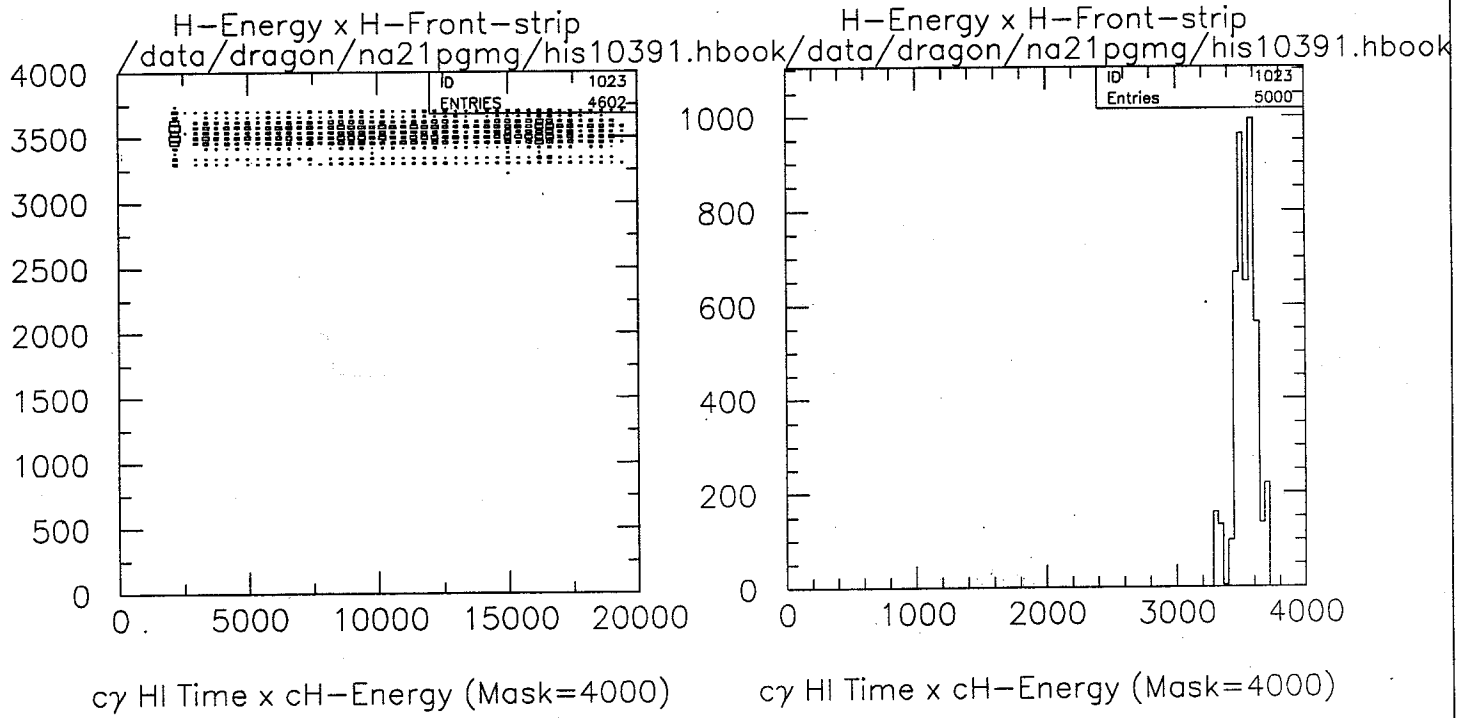
L7 - TRI0756 "EL prescaler" produces an output every Nth trigger of the elastic SCA, described above. N is selected manually by a front panel rotary switch which displays the base-2 log of N i.e. N=2**(switch setting). The prescale factor reduces the number of elastic triggers which are acquired, for the purpose of rejecting noise or saving disc space or reducing elastic dead-time, which is also the deadtime of the end-detector.

L8/L9/l10 - LRS612A "fast amplifiers" linearly amplify the gamma-array anode pulses from 70% output of the "resistive splitters". Each NIM station contains a module with 12 independent gain=10 amplifiers, one for each of the 30 gamma detectors. Some of the spare 6 amplifiers have been substituted for bad channels among the first 30 channels of the 36 available channels. Each amp has two independent outputs; one goes via filters to the gamma CFD's in C1/C2 and one goes to the gamma LED's in C3/C4.

L11 - BNCBH-1 "gamma triggered pulser" is a double-width pulser which can be used to drives the front-16 strip preamps via a common input connector on the preamp box. For normal acquisition this pulser should be turned off by its panel switch. The following-page paw spectra were made with DSSSD BIAS ON and sliding the pulser delay to simulate all possible gamma-end time differences. The pulser is also useful for testing the acquisition into the H memory. The scope picture below was made from the WSO output of the H memory driver at C22. The WSO pulses (middle trace) are more complicated than the pulser ones shown above. This time there are 20 words of ADC data transferred in two groups. Each group has 2 headers and 8 data words, one datum from each strip.

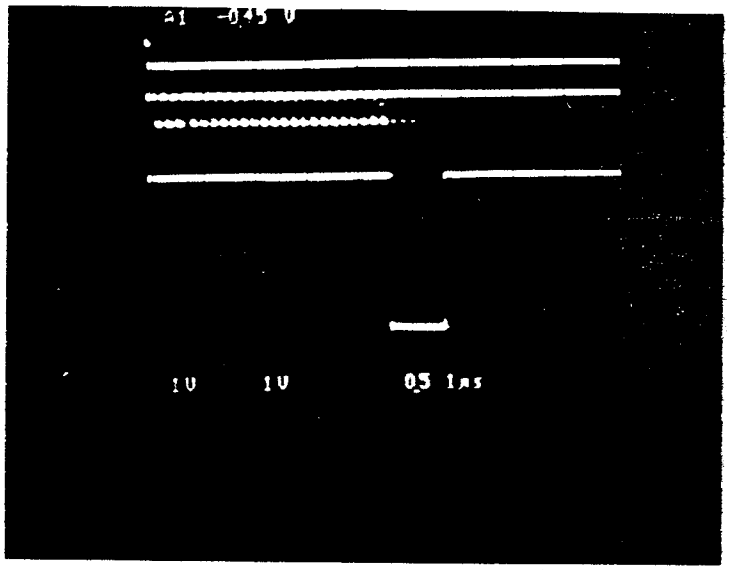
2003/12/19 14.39





cγ HI Time x cH−Energy (Mask=4000)

cγ HI Time x cH−Energy (Mask=4000)



E3/E4 - RAL "front amp/disc" 8-channel Eurocrate modules shape and discriminate the signals from the RAL preamps. A 75' multi-conductor bundle connects the preamp box at the end-detector to the amp/disc modules in the "overflow" rack near the target. Also in the bundle are power and pulser input to the preamps. The amp/disc modules are powered by 5 separate DC power modules above the crate. Power-on is indicated by green lights on each power module. The power supplies are protected by a line-fuse in a pop-out connector on the back panel of the crate. Spare fuses are in a plastic bag taped to the back panel nearby. The discriminator levels are adjusted by screwdriver pots on the front panels, one pot for each 8-channels. The discriminator level is normally set to 50mV as indicated by a red testpoint on the front panels. Shielded 8-conductor multi-cables go to H ADC's and a 16-conductor cable to a logic fanin to form the end-detector trigger.

E5/E6 - RAL "back disc" are modules identical to those described above, but driven by a separate 16-conductor cable from the back DSSSD strip preamps. A 16-conductor output cable goes to a 16-conductor flat delay-cable and then to the first 16 H TDC stop inputs.

midmes01:/home/dragon/online/daqelectronics.doc

Joel Rogers
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DRAGON DAQ ELECTRONICS